

WHAT IS CLAIMED IS:

1 *Sub*
2 *a* 1. An M-bit adder capable of receiving a first M-bit
3 comprising:

4 M adder cells arranged in R rows, wherein a least
5 significant adder cell in a first one of said rows of adder cells
6 receives a first data bit, A_x , from said first M-bit argument and
7 a first data bit, B_x , from said second M-bit argument, and
8 generates a first conditional carry-out bit, $C_x(1)$, and a second
9 conditional carry-out bit, $C_x(0)$, wherein said $C_x(1)$ bit is
10 calculated assuming a row carry-out bit from a second row of adder
11 cells preceding said first row is a 1 and said $C_x(0)$ bit is
12 calculated assuming said row carry-out bit from said second row is
13 a 0.

1 2. The M-bit adder as set forth in Claim 1 wherein said
2 least significant adder cell generates a first conditional sum bit,
3 $S_x(1)$, and a second conditional sum bit, $S_x(0)$.

1 *pat* 3. The M-bit adder as set forth in Claim 2 wherein said
2 $S_x(1)$ bit is calculated assuming said row carry-out bit from said
3 second row is a 1 and said $S_x(0)$ bit is calculated assuming said
4 row carry-out bit from said second row is a 0.

1 4. The M-bit adder as set forth in Claim 3 wherein said row
2 carry-out bit selects one of said $S_x(1)$ bit and said $S_x(0)$ bit to
3 be output by said least significant adder cell.

1 5. The M-bit adder as set forth in Claim 4 wherein said
2 first row of adder cells further comprises a second adder cell
3 coupled to said least significant adder cell, wherein said second
4 adder cell receives a second data bit, A_{x+1} , from said first M-bit
5 argument and a second data bit, B_{x+1} , from said second M-bit
6 argument, and receives from said least significant adder cell said
7 $C_x(1)$ bit and said $C_x(0)$ bit.

1 *Pat* 6. The M-bit adder as set forth in Claim 5 wherein said
2 second adder cell generates a first conditional carry-out bit,
3 $C_{x+1}(1)$, wherein said $C_{x+1}(1)$ bit is generated from said A_{x+1} data bit,
4 said B_{x+1} data bit, and said $C_x(1)$ bit from said least significant
5 adder cell.

1 7. The M-bit adder as set forth in Claim 6 wherein said
2 second adder cell generates a second conditional carry-out bit,
3 $C_{x+1}(0)$, wherein said $C_{x+1}(0)$ bit is generated from said A_{x+1} data bit,
4 said B_{x+1} data bit, and said $C_x(0)$ bit from said least significant
5 adder cell.

1 8. The M-bit adder as set forth in Claim 7 wherein said
2 second adder cell generates a first conditional sum bit, $S_{x+1}(1)$,
3 wherein said $S_{x+1}(1)$ bit is generated from said A_{x+1} data bit, said
4 B_{x+1} data bit, and said $C_x(1)$ bit from said least significant adder
5 cell.

1 *Sub* 9. The M-bit adder as set forth in Claim 8 wherein said
 2 *ai* second adder cell generates a second conditional sum bit, $S_{x+1}(0)$,
 3 wherein said $S_{x+1}(0)$ bit is generated from said A_{x+1} data bit, said
 4 B_{x+1} data bit, and said $C_x(0)$ bit from said least significant adder
 5 cell.

1 10. The M-bit adder as set forth in Claim 9 wherein said row
 2 carry-out bit selects one of said $S_{x+1}(1)$ bit and said $S_{x+1}(0)$ bit to
 3 be output by said second adder cell.

1 11. The M-bit adder as set forth in Claim 1 wherein said
 2 first row of adder cells contains N adder cells and said second row
 3 of adder cells preceding said first row contains less than N adder
 4 cells.

1 *Sub*
2 *Pat*
12. A data processor comprising:

3 an instruction execution pipeline comprising N processing
4 stages, each of said N processing stages capable of performing one
5 of a plurality of execution steps associated with a pending
6 instruction being executed by said instruction execution pipeline,
7 wherein at least one of said N processing stages comprises an M-bit
8 adder capable of receiving a first M-bit argument, a second M-bit
9 argument, and a carry-in (CI) bit, said M-bit adder comprising:

10 M adder cells arranged in R rows, wherein a least
11 significant adder cell in a first one of said rows of adder
12 cells receives a first data bit, A_x , from said first M-bit
13 argument and a first data bit, B_x , from said second M-bit
14 argument, and generates a first conditional carry-out bit,
15 $C_x(1)$, and a second conditional carry-out bit, $C_x(0)$, wherein
16 said $C_x(1)$ bit is calculated assuming a row carry-out bit from
17 a second row of adder cells preceding said first row is a 1
18 and said $C_x(0)$ bit is calculated assuming said row carry-out
bit from said second row is a 0.

1 *Sub*
2 *ai* 13. The data processor as set forth in Claim 12 wherein said
3 least significant adder cell generates a first conditional sum bit,
4 $S_x(1)$, and a second conditional sum bit, $S_x(0)$.

1 14. The data processor as set forth in Claim 13 wherein said
2 $S_x(1)$ bit is calculated assuming said row carry-out bit from said
3 second row is a 1 and said $S_x(0)$ bit is calculated assuming said
4 row carry-out bit from said second row is a 0.

1 15. The data processor as set forth in Claim 14 wherein said
2 row carry-out bit selects one of said $S_x(1)$ bit and said $S_x(0)$ bit
3 to be output by said least significant adder cell.

1 16. The data processor as set forth in Claim 15 wherein said
2 first row of adder cells further comprises a second adder cell
3 coupled to said least significant adder cell, wherein said second
4 adder cell receives a second data bit, A_{x+1} , from said first M-bit
5 argument and a second data bit, B_{x+1} , from said second M-bit
6 argument, and receives from said least significant adder cell said
7 $C_x(1)$ bit and said $C_x(0)$ bit.

1 *Sub* 17. The data processor as set forth in Claim 16 wherein said
2 second adder cell generates a first conditional carry-out bit,
3 $C_{x+1}(1)$, wherein said $C_{x+1}(1)$ bit is generated from said A_{x+1} data bit,
4 said B_{x+1} data bit, and said $C_x(1)$ bit from said least significant
5 adder cell.

1 18. The data processor as set forth in Claim 17 wherein said
2 second adder cell generates a second conditional carry-out bit,
3 $C_{x+1}(0)$, wherein said $C_{x+1}(0)$ bit is generated from said A_{x+1} data bit,
4 said B_{x+1} data bit, and said $C_x(0)$ bit from said least significant
5 adder cell.

1 19. The data processor as set forth in Claim 18 wherein said
2 second adder cell generates a first conditional sum bit, $S_{x+1}(1)$,
3 wherein said $S_{x+1}(1)$ bit is generated from said A_{x+1} data bit, said
4 B_{x+1} data bit, and said $C_x(1)$ bit from said least significant adder
5 cell.

1 *sub* 20. The data processor as set forth in Claim 19 wherein said
2 *part* second adder cell generates a second conditional sum bit, $S_{x+1}(0)$,
3 wherein said $S_{x+1}(0)$ bit is generated from said A_{x+1} data bit, said
4 B_{x+1} data bit, and said $C_x(0)$ bit from said least significant adder
5 cell.

1 21. The data processor as set forth in Claim 20 wherein said
2 row carry-out bit selects one of said $S_{x+1}(1)$ bit and said $S_{x+1}(0)$
3 bit to be output by said second adder cell.

1 22. The data processor as set forth in Claim 12 wherein said
2 first row of adder cells contains N adder cells and said second row
3 of adder cells preceding said first row contains less than N adder
4 cells.

Pat
23. A method of adding a first M-bit argument and a second M-bit argument in an M-bit adder, the M-bit adder comprising M adder cells arranged in R rows, the method comprising the steps of:

receiving a first data bit, A_x , from the first M-bit argument and a first data bit, B_x , from the second M-bit argument in a least significant adder cell in a first one of the rows of adder cells;

calculating in the least significant adder cell a first conditional carry-out bit, $C_x(1)$, assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1;

calculating in the least significant adder cell a second conditional carry-out bit, $C_x(0)$, assuming the row carry-out bit from the second row is a 0;

calculating in the least significant adder cell a first conditional sum bit, $S_x(1)$, assuming the row carry-out bit from the second row is a 1;

calculating in the least significant adder cell a second conditional sum bit, $S_x(0)$, assuming the row carry-out bit from the second row is a 0;

propagating the $C_x(1)$ bit and the $C_x(0)$ bit to a second adder cell in the first row of adder cells; and

selecting one of the $S_x(1)$ bit and the $S_x(0)$ bit to be

ATTY. DOCKET NO. 00-C-050

PATENT

~~output from the least significant adder cell according to a value of the row carry-out bit from the second row.~~

| Year | 1977 | 1978 | 1979 | 1980 | 1981 | 1982 | 1983 | 1984 | 1985 | 1986 | 1987 | 1988 | 1989 | 1990 | 1991 | 1992 | 1993 | 1994 | 1995 | 1996 | 1997 | 1998 | 1999 | 2000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 | 2032 | 2033 | 2034 | 2035 | 2036 | 2037 | 2038 | 2039 | 2040 | 2041 | 2042 | 2043 | 2044 | 2045 | 2046 | 2047 | 2048 | 2049 | 2050 | 2051 | 2052 | 2053 | 2054 | 2055 | 2056 | 2057 | 2058 | 2059 | 2060 | 2061 | 2062 | 2063 | 2064 | 2065 | 2066 | 2067 | 2068 | 2069 | 2070 | 2071 | 2072 | 2073 | 2074 | 2075 | 2076 | 2077 | 2078 | 2079 | 2080 | 2081 | 2082 | 2083 | 2084 | 2085 | 2086 | 2087 | 2088 | 2089 | 2090 | 2091 | 2092 | 2093 | 2094 | 2095 | 2096 | 2097 | 2098 | 2099 | 2100 |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 1977 | 1978 | 1979 | 1980 | 1981 | 1982 | 1983 | 1984 | 1985 | 1986 | 1987 | 1988 | 1989 | 1990 | 1991 | 1992 | 1993 | 1994 | 1995 | 1996 | 1997 | 1998 | 1999 | 2000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 | 2032 | 2033 | 2034 | 2035 | 2036 | 2037 | 2038 | 2039 | 2040 | 2041 | 2042 | 2043 | 2044 | 2045 | 2046 | 2047 | 2048 | 2049 | 2050 | 2051 | 2052 | 2053 | 2054 | 2055 | 2056 | 2057 | 2058 | 2059 | 2060 | 2061 | 2062 | 2063 | 2064 | 2065 | 2066 | 2067 | 2068 | 2069 | 2070 | 2071 | 2072 | 2073 | 2074 | 2075 | 2076 | 2077 | 2078 | 2079 | 2080 | 2081 | 2082 | 2083 | 2084 | 2085 | 2086 | 2087 | 2088 | 2089 | 2090 | 2091 | 2092 | 2093 | 2094 | 2095 | 2096 | 2097 | 2098 | 2099 | 2100 | |